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5 kW SLEEPS INVERTER

FINAL TECHNICAL REPORT

DATA ITEM A-001

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D. W. Shireman, I. J. Millman, C. L. Doughman

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SECTION I
SUMMARY

The objective of this program was to develop a preprototype 5 kW inverter capable of operating from a fuel cell source of 36 to 60 volts DC. The output characteristics of the inverter are selectable for the following configuration; single-phase 120 volts AC, split-phase 120/240 volts AC, and three-phase 120/208 volts AC. The output frequency may be either 60 Hz or 400 Hz.

The effort has resulted in a preprototype unit capable of supplying the required output voltages, frequencies, and current. The preprototype consists of two packages, the inverter and remote control head with interconnecting cable.

The work described in this report is authorized under MERADCOM CONTRACT DAAK70-79-C-0149. The work completed and documented here is Contract Data Item Number 001, Scientific and Technical Reports Type III Final. The design information was incorporated into the final design of the 5 kW inverter preprototype which was delivered to MERADCOM.

The primary authors of this report are D. W. Shireman, I. J. Millman, and C. L. Doughman.

SECTION II
INTRODUCTION

This program covers the development of a universal preprototype 5 kW inverter for use with a fuel cell source. The inverter is to be capable of operating at either 60 Hz or 400 Hz output frequency. This feature is controlled by a manual switch on the external surface of the unit.

The output may be configured in any of the following three ways: 1-phase 120 volts Ac, split-phase 120/240 volts AC, or 3-phase 120/208 volts AC. This feature is controlled by a rotary switch on the external surface of the unit. These functions are interlocked by a switch on the cover to shutdown the unit.

The inverter is packaged in an enclosure 34 inches long, 19 inches wide, and 9.75 inches high. The enclosure is forced air cooled with drip proof covers and the unit weighs 165.5 pounds.

A remote control and instrument head enclosure contains the output current and voltage meters, fault indicator and mode of operation indicators. It is 7 inches high, 6.5 inches wide, and 4 inches deep and weighs 5.5 pounds.

A preprototype unit was constructed and tested. System interface problems were encountered when the inverters and booster sections were operated together in the chassis and an extended effort was applied to this phase, investigating the causes and solutions to all the noise problems. The problems were reduced to a minimum and the unit tested and shipped.

SECTION III
SYSTEM DESCRIPTION

3.0 General

Westinghouse has designed a two-stage power conversion system. A DC-DC converter is used on the input to create three isolated 200 VDC-Links, and a transformerless, single-phase, inverter module is connected to each link. The outputs of these three inverter modules can be arranged in three configurations and operated at either 60 or 400 Hz.

3.1 System Block Diagram

Figure 3-1 is the system block diagram. A brief description of the system segments follows.

The input filter has been designed to attenuate the ripple current produced by the booster modulating frequencies to the levels allowed by MIL-STD-461. These low levels are more than adequate with respect to the fuel cell power plant, which is sensitive to ripple current.

The control circuits of the inverter modules are referenced to the AC output neutral and are powered by a switching DC-DC power supply. In addition, the supply will power the booster controls, which are referenced to DC minus, by a separate set of isolated outputs. The power supply has built in protection for failures (which could result in damage to the other control components) due to overvoltage.

Booster Regulator

The booster regulator is the largest power handling module in the system. It converts all of the 36-60 volt DC input energy to three separate isolated 200 volt DC-Links which are connected to the three inverter modules.

The DC-DC converter is a dual interlaced flyback conversion circuit. Transformers and associated rectifiers and capacitors provide the three 200 volt DC-Link outputs. Voltage control of the booster output is achieved by means of high impedance differential amplifier feedback from the DC-Links to the active control circuit. The power switches are pulse width modulated (PMW) such that the average of the three DC-Links is 200 volts. Protection circuits monitor link voltages, peak currents and the start/stop sequencing of the inverter.

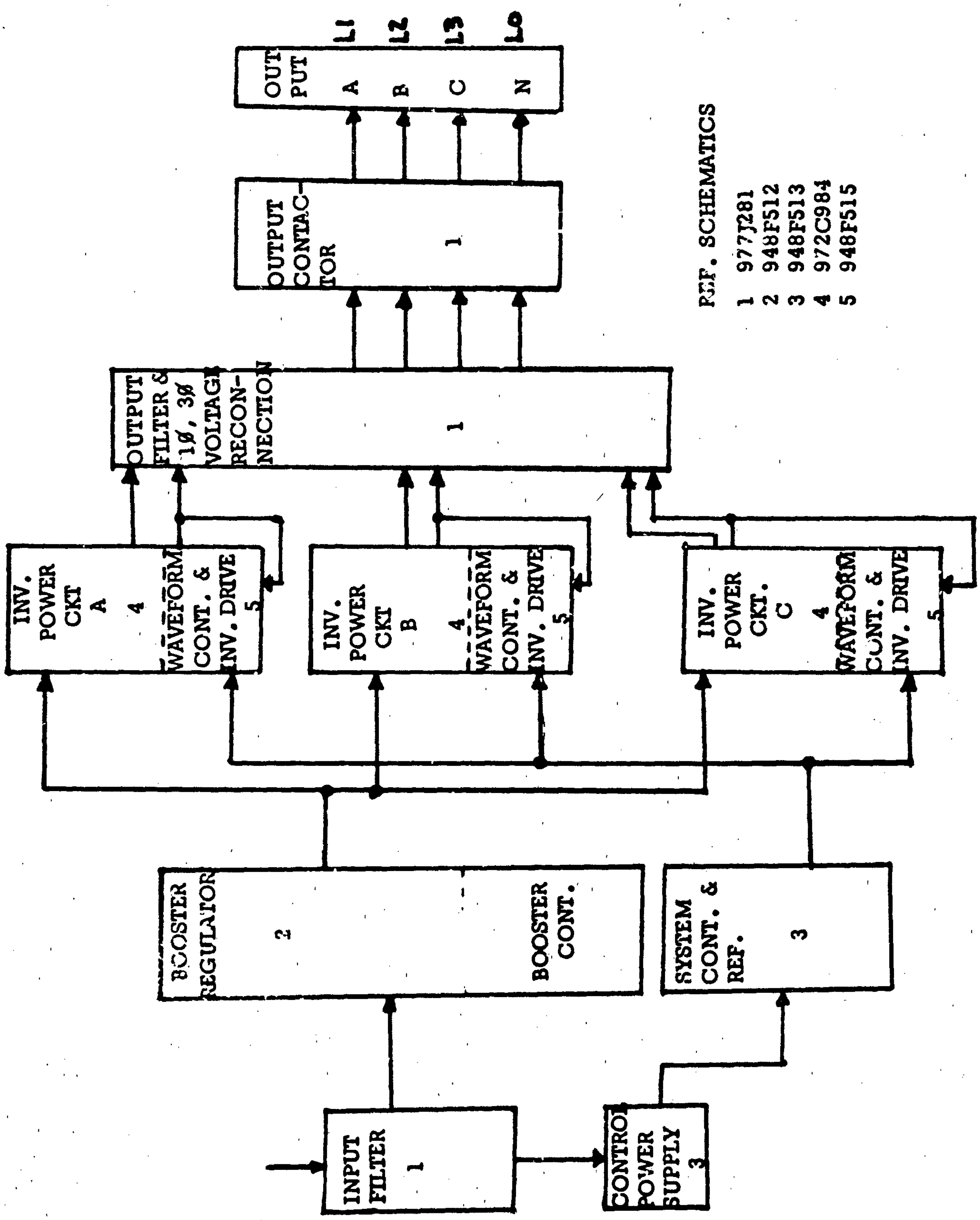


Figure 3-1
System Block Diagram

Booster Regulator (Continued)

Because the two booster power circuits are connected in parallel, small variations in circuit impedances and transistor switching times cause large current unbalances. An active current balancing feedback loop is used to force current balance. An error signal is derived by determining the difference in peak currents in the primary switching circuits. This error signal modifies the average voltage regulation signal to shorten the on-pulse of the too-high current and to lengthen the on-pulse of the too-low current. Thus the peak current difference is reduced toward zero.

In our efforts to eliminate the noise problems in the booster, while maintaining high frequency response and loop stability, many design changes were made.

Positive hysteresis feedback was applied to the triangle reference, DC level comparator, to generate a noise immunity band immediately after the turn on pulse of a power pole. The noise is generated by the inverter switching which is not synchronized with the booster.

The booster frequency response was stabilized by adding a lead network to cancel out one of the lags due to the DC-Link filters. The lead network provides 20 dB per decade gain beginning at about 30 Hz. This improved the stability but the reflected inverter noise again posed a problem. Additional lags beyond 500 Hz were added to reduce this high frequency noise. The calculated frequency response curve (Bode Plot) is shown in Figure 3-2. Measurements made on the unit indicate that the actual response is very close to the calculated response.

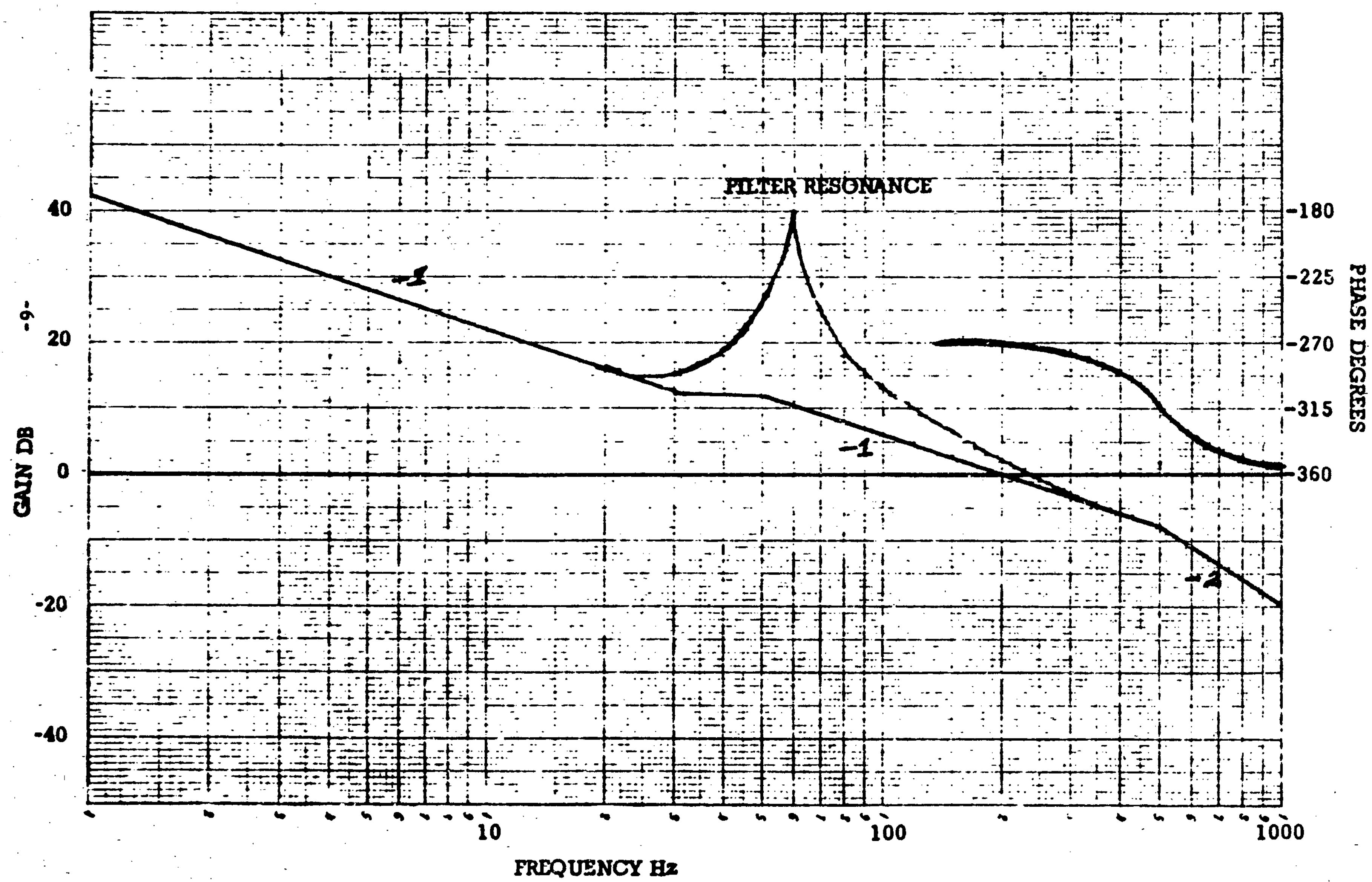
Inverter Module

Three independent, single-phase inverters individually convert the DC-Link voltages to either 60 or 400 Hz AC power. The power output is achieved by pulse-width modulation and by Staggered-Phase, Carrier-Cancellation techniques.

Attempts to reduce the waveform distortion with feedback circuits were not successful. The largest contributor to this distortion is the time lag (under lap) in the two pole transistors. The underlap is necessary to prevent the pole from short circuiting the DC Link. The results of this work are given in Appendix A.

A 3,600 Hz triangle waveform provides the modulation signal for the PWM waveform and voltage regulation control circuits. Three sinewave voltage references are also generated. These may be either 60 Hz or 400 Hz. The phase relationship of these sinewaves is selected to provide single-phase or three-phase power to the loads.

Figure 3-2
CALCULATED
BOOSTER LOOP RESPONSE CURVE
INCLUDING FILTER RESONANCE



Inverter Module (Continued)

The waveforms described above are combined to generate the PWM control for each leg of the single-phase bridge inverter. Should the peak current out of the inverter exceed rated current, the waveform control PWM signals are overridden by a current limiting control circuit. Peak current is detected and locks out the PWM signals such that the load current is circulated within the inverter bridge preventing further current increase. When the current decreases to the lower hysteresis level of the current limiting control circuit, the waveform control circuit resumes control of the power switches. The power transistors in the inverter bridge are switched by the controlled current feedback transformers (CCFT).

The CCFT's in turn are controlled by the amplified PWM signals from nand gates. The CCFTs provide efficient base drive because the base drive is directly proportional to output load current. Only low-level control signals are required.

Output Filter and Reconnection

The output of each single-phase inverter module is connected to a low-pass, L-C filter. The filter is sized to attenuate the harmonics from the PWM inverter.

The reconnections necessary to provide the various output voltage and phase relationships are accomplished with a control switch.

3.2 System Output Capabilities

The system output parameters with respect to voltage and frequency requirements are met in total. Additional capability is provided when the unit is connected to provide a single-phase output. These capabilities are summarized below.

Three-Phase

When connected in a three-phase array, the outputs can be either 60 or 400 Hz and support a load on the four wire 120/208 output of 6250 VA at .8PF with overload capability at 1.2 per unit. Each inverter module is independently controlled.

Single-Phase

The output may be connected as a three-wire 120/240 volt single-phase source, as a 240 volt two-wire single-phase source, or as a 120 volt two-wire single-phase source. The load frequency may be either 60 Hz or 400 Hz.

Single-Phase (Continued)

The 120/240 volt connection connects two inverter modules in series. The sinewave references are phase shifted 180 degrees. Each module is independently controlled. The two modules provide 6 kVA at .8PF. The third inverter module is loaded by the internal cooling fans. Peak transistor current is limited to 42 amperes. Load terminals L1 to Lo provide over 120 volt to neutral output and L2 to Lo provide the other. A 240 volt load may be connected between terminals L1 and L2.

Two inverter modules are paralleled to supply 6 kVA 0.8PF at 120 volts. Phase A and Phase B modules are connected in parallel and phase A control circuits take over the PWM generation for both modules. This configuration requires no active paralleling loops. Load connection is made by paralleling terminals L1 and L2 for one side and Lo (neutral) for the other.

3.3 System Operational Details

Booster Regulator Module

The function performed by the booster regulator module is to transform the variable DC input (36 to 60 volts) to three isolated 200 volt DC-Links. The isolated DC-Links are used as the source for the three inverter modules.

The main power switches in the conversion circuits are arranged in two sets of three transistors. The three transistors are matched for gain (hfe) at a collector current of 20 amperes.

Power connection from each paralleled transistor emitter to the common bus is utilized to force the impedance of the current sharing. By paralleling three transistors, the saturation losses are kept low to help meet the efficiency objectives. The power transistor selected is the Westcode WT5516 which has 300 amperes peak capability, and 200 amperes continuous. This yields a capability of 900 amperes peak and 600 amperes continuous for the three. The peak operating current in the circuit is 250 amperes allowing ample margin.

The power switches are pulse width modulated by the regulator circuits through Controlled Current Feedback Transformers (CCFTs). Each set of transistors, transformer, and diodes forms a flyback power circuit. Two flyback circuits are interlaced to form an apparent full wave converter at the filter (link) capacitors.

The CCFT's are controlled by power field-effect transistors (FETs) which provide low loss, fast switching to improve efficiency. The pulse width modulated signal is coupled to the power FETS by a dual driver IC, (Siliconix D160).

The three isolated outputs of the flyback power circuit are sensed by differential amplifiers. The average of these voltages provide a feedback signal which is compared to a DC reference voltage at the input to the error amplifier. The output of the error amplifier is compared with a saw-tooth wave to provide the pulse width modulated signal. Digital logic is used to split the pulses to form the interlace signals for the power circuits.

Booster Regulator Module (Continued)

Both self and system protection features are provided in the Booster Control. Peak current in each power circuit is monitored and the conduction period is foreshorted and the switching frequency increased when the current limit level is exceeded. Should current increase beyond the current limit level, an overcurrent fault signal stops the inverter requiring a manual reset. Similarly, an overvoltage on the DC-Link and an input voltage lower than 35 volts also stops the inverter requiring manual reset.

Inverter Modules

The inverter modules convert the DC-Link voltage of 200 volts DC to either 60 hertz or 400 hertz AC as determined by the operator. These modules are required to develop either a single-phase or a three-phase power source.

The four main power switches of each inverter module are connected in a single-phase, full wave bridge arrangement. The switches are pulse width modulated to obtain both output voltage regulation and waveform harmonic reduction. The output of each bridge is connected to a low pass L-C filter to reduce the PWM ripple voltages. Solitron SDT96306 transistors are used for the power switches.

The PWM drive signals are developed by comparing a high quality sinewave reference voltage of the desired output frequency to a high frequency (3600 hertz) triangle modulating signal. The null points of these two signals determine the on-off ratio of two of the bridge transistors which alternately connect one output terminal to the plus DC-Link voltage and to the minus DC-Link voltage. The two output terminals (AC and Neutral) are modulated out of phase such that the basic 3600 hertz ripple frequency is cancelled.

The amplitude of the sinewave reference voltage is controlled by a DC feedback loop. The logic senses and rectifies the output voltage; compares this voltage to a DC reference and adjusts the magnitude of the reference such that the output voltage is nominally 120 volts.

3.4 5 KW Inverter, General Description

The MERADCOM 5 kW preprototype inverter described herein is a weather proof module having the overall maximum dimensions of 9.75, by 19 by 34 inches, representing a 6300 cubic inch volume and weighs 165.5 pounds.

The rear of the inverter incorporates an input DC terminal block. A 32 pin connector is also incorporated at the rear for connection to the control instrumentation head via a 5 foot cable. A louvered plate is incorporated on the inside of the back wall for the exit of cooling air. The perimeter of this plate is gasketed to prevent water leakage into the unit.

3.4 5 KW Inverter, General Description (Continued)

The base or bottom of the inverter is completely flat. The two 9.75 by 34 inch side surfaces are flat. The top of the inverter is a .093-inch thick aluminum panel with 25 cross-recessed-head, quarter-turn, fasteners mating with blind receptacles on the inside flanges of the box.

The MERADCOM inverter control head is a weather proof module having overall maximum dimensions of 4.00 x 6.5 x 7.00 inches. The weight of the control head is 5.5 pounds, less the interconnect cable.

All instrumentation and operating components are mounted on a bezel which is recessed into an aluminum box forming the rear cover. The rear cover is attached using four mounting screws, accessible from the front bezel. A rear mounted 32 pin connector interconnects the two units.

3.5 Waste Heat Dissipation

Waste heat from the 5 kW Inverter is removed by forced air provided by two 400 Hz/60 Hz fans. Cooling air is drawn in via a front mounted louver and filter assembly, and flush air cools the front third of the chassis. The air then passes into a longitudual distribution duct, and is directed onto the Inverter and booster heat sinks through appropriately sized apertures. After flowing across the heat sinks, the air is collected in a plenum on the opposite side of the chassis. The air is then distributed into the rear third of the chassis to flush cool the rest of the booster. Exhaust air leaves the cabinet via a rear mounted drip proof louvered plate.

The present cooling system is not adequate to cool the inverter when configured for 400 Hz operation. An improved forced air cooling arrangement is required. Fan connections are provided to allow powering of the fans from an external 60 Hz source when the inverter is configured for 400 Hz operation. When powered from a 60 Hz, 120V RMS supply, the fans provide adequate cooling at ambient air temperatures up to 40°C.

SECTION IV
SYSTEM DESIGN, DEVELOPMENT AND TESTING

4.1 Design and Development

Following design submission to MERADCOM in September 1980, a major effort was undertaken to investigate and eliminate the 400 Hz harmonic distortion which appeared in the Inverter outputs. In conjunction with this effort, integral error control and feedback circuit instablities were also analyzed. Ultimately, these problems were substantially solved and by April 1981, a final design configuration for the inverter controls and power stage had been determined. The system control design had already been prepared in detail, and bread board mock-ups gave good results.

MERADCOM design approval was received in November 1980 and mechanical design of the chassis, mounting components and cooling system was commenced. At this time, concern was expressed regarding the effectiveness of the cooling fan design, and the acoustic noise generated. Tests were undertaken which resulted in an acceptable design by March 1981. The chassis design proceeded smoothly, and the chassis was fabricated without significant changes. Attention was also given to EMI radiation and susceptibility at this time.

In January 1981, design of the Low Voltage Power Supply was started, together with the Start/Stop system. These items were completed by March 1981.

Fianl design of the Booster and its controls was completed in March 1981. At that time, some question arose as to the efficiency of the Booster, and design changes were incorporated as a result of development work. The Booster design was completed in May 1981.

4.2 Fabrication/Debugging

Fabrication of the system components commenced in January 1981. The Booster was completed in August and the Inverter boards in September, 1981.

Debugging and fault finding in each of the system components immediately followed fabrication. The Booster efficiency was below design specification, but work carried out between March and August 1982 brought the figure up to a satisfactory 90 percent.

4.2 Fabrication/Debugging (Continued)

The Inverter boards also caused initial problems due to instability and low power capacity. Work carried out between August and November 1981 solved these problems.

In December 1981, system integration was completed and debugging of the entire system commenced. After overcoming some initial problems caused by interaction between the Booster and Inverter, the entire system was demonstrated to MERADCOM personnel in January 1982.

4.3 Feasibility Testing/Demonstration

In April 1982, a feasibility testing program was launched whose objectives included a formal performance demonstration of the system to MERADCOM.

Several problems arose during initial stages of the testing program. Spurious pulses in the inverter outputs, noise and/or modulation on reference signal lines (especially the 7200 Hz triangle wave) and grounding/shielding/interference effects were encountered when the entire equipment was run in the chassis. These problems were found to be inter-related and, together with a deficient performance from the power supply, required two months of intensive work during April and May 1982.

Two other problem areas had also been successfully dealt with during this time. The Start/Stop system which brings the system into operation and shuts it down in an orderly fashion had presented persistent problems. These were solved one by one and this system now operates consistently well. The cooling fans were originally configured to operate in parallel at 60 Hz, and with one fan disabled at 400 Hz, in order to minimize acoustic noise. Subsequent tests revealed that operation in parallel at both frequencies provided better cooling without significant increase in acoustic noise.

By June 1982, the entire system had been run at full power in all three selectable output modes, both at 400 Hz and 60 Hz. The power supply capacity and performance was still in doubt, and a reconfiguration was carried out at this time in order to clear up this problem. Delays caused by this redesign/reconfiguration eventually led to the postponement of the formal performance test demonstration until later in the year.

4.4 Summary of Preprototype Debugging and Testing

The booster power and control boards were installed in the enclosure. Resistive loads were connected to the DC outputs. The input was applied and the problems of stability and noise pulses resolved.

The inverter modules were tested on the bench and circuit problems resolved. The inverter modules were installed one at a time into the enclosure. As inverter modules were added noise problems with the booster and between inverter modules increased. Noise isolation had to be built into the circuits to allow the booster and inverters work in concert. Shielded wires, decoupling capacitors and increased hysteresis feedback were explored.

The problems associated with the distortion in the output waveform were investigated the results presented in Appendix A.

The preprototype unit was tested and shipped to MERADCOM where it was demonstrated that the booster stability was marginal when the unit was connected to a H.P. regulated supply through an L-C filter. The unit was returned to Westinghouse and the loop response modified as presented in this report.

Test data is provided in a separate report, Data Item 003. Tests include transient and steady state response, temperature run, balanced and unbalanced loading.

SECTION V
RECOMMENDATIONS

5.1 General

The following are recommendations for improvement in the design of the preprototype units for future generations of this type of power converter. Some of these recommendations have already been implemented (as noted by*) in the 5 kW preprototype as part of the recent efforts to improve its nominal performance envelope.

5.2 Shielding/Wiring/Grounding

Any wire carrying pulse type signals should be shielded, or if its return can be separated, a twisted pair should be used. When in doubt, twisted shielded wires may be used with advantage.

All signals entering or leaving the PWM generating system must be shielded, particularly reference signals.* This recommendation applies particularly to the motherboard where signals frequently cross each other, or run parallel for some length*.

Cable bundles running the entire length of the Chassis must also be shielded, particularly those required to continue on to the Control Head.* The optimum point to ground this shield needs to be established.

Every effort must be made to avoid wire loops commencing at, and returning to, the Waveform Control Board, especially when they extend as far as the Control Head*.

A ground plane between the Inverter Controls and the CCFTs is recommended, and also Faraday shields on each CCFT.

Each Inverter Board was grounded separately to system neutral in order to keep the ground as short as possible*. This introduces the possibility of ground loops, but does not seem to cause problems in this case. An investigation of the best configuration is recommended.

5.3 Triangle Waveform Generator

Initially the active device in the signal generator was referenced to the +15V Inverter supply. Difficulties with ripple and noise voltages required a separate Zener supply, and substantial decoupling of active modes. Finally, the solution adopted was to reference the generator to the -6.4V reference line. This line is now shielded and has very little fluctuating load, thus providing a stable reference even in the presence of substantial output voltage transients.

5.4 Power Supply

One of the major sources of interference and noise spikes is the Power Supply, especially since its frequency is not related to the Inverter PWM frequency (7200 Hz) and it varies with load. It is recommended that the Power Supply be operated as a variable duty cycle, constant frequency unit. The frequency of operation should be derived from the crystal. In this way, any switching transients generasted in the Power Supply could only produce non time-dependent anomalies in the triangle waveform or phase reference outputs. The switching power supply should be located remote from the control circuits.

5.5 Control Head

This unit itself caused very few problems during the three months of this investigation. Two recommendations are:

a. Lamp bulb should be changed from the unnecessarily large 150 mA types to the 40 or 50 mA type.*

b. In order to provide remote output voltage adjustment, the -6.4V ref signal was taken from the Waveform Control board to the Control Head, through a potentiometer, and then returned to Inverter Ground on the Waveform Control Board. This line had to be disabled in order to prevent large spurious signals from appearing in the PWM output. If this remote adjustment is mandatory, some form of isolation must be provided between the adjustment potentiometer and the Waveform Control Board.

5.6 Faraday Shields

In order to improve isolation between the control signals and Inverter outputs, it is recommended that Faraday shields be applied to all four CCFT's in each Inverter board. Substantial improvements in feedback stability should be achieved using this technique.

5.7 Mechanical Layout

During the course of the program, several points arose which form recommendations for future design.

a. The motherboard should be designed so that it may be easily removed and replaced, particularly without removal of other major electrical components.

b. Longitudinal, rather than transverse, stiffeners should be integral with the motherboard*.

c. The Inverter Board control and Power board interface should be designed to provide far greater rigidity and ease of disassembly.

5.8 Reliability/Maintainability

In order to improve the reliability/maintainability aspects of the equipment, recommendations for future development are made.

a. Printed circuit techniques should be employed where possible particularly for the Inverter Boards and Booster Controls.

b. Test Points should be provided to enable fault diagnosis and performance appraisal to be carried out without removal of any component or assembly from the chassis.

c. Circuits should be designed to minimize the effect of loss of one or more control signals, and provide an orderly shutdown following loss of a regulated bus.

5.9 BITE/Simulator

One of the major difficulties experienced in establishing the performance of the system lay in ensuring that each sub-assembly was operating correctly. Recommendations for future systems of this type are:

a. Some form of Built-In-Test Equipment (BITE) should be incorporated in the design to aid in fault diagnosis.

b. A simulator capable of accommodating all circuit boards should be built. This simulator would provide appropriate power and signal inputs, and sense circuit board outputs so that the operational effectiveness of each circuit may be quickly established. The simulator itself should be capable of a range of outputs so that the effects of different circuit parameters may be ascertained.

5.10 Cooling

The large pressure head loss at the fan inlet causes the low flow into the unit. A centrifugal blower will be required to deliver the necessary volume of air to cool the unit should the present thickness of air filter be maintained. Note that a centrifugal blower will increase noise levels significantly over those of the saucer fan now used. A preferable option is to replace the present air filter with one that has less head loss across it. The louvered panels should have increased open area to aid the flow. In addition, some components need larger heat sinks to increase cooling with the quiet tubeaxial-saucer fan. Since the available multiple frequency fans do not provide adequate flow at both frequencies, a fixed frequency inverter driven fan from the input source is preferred.

5.11 Booster

The booster efficiency is given as 90 percent in Paragraph 4.2 with a resistive load and supplying direct current.

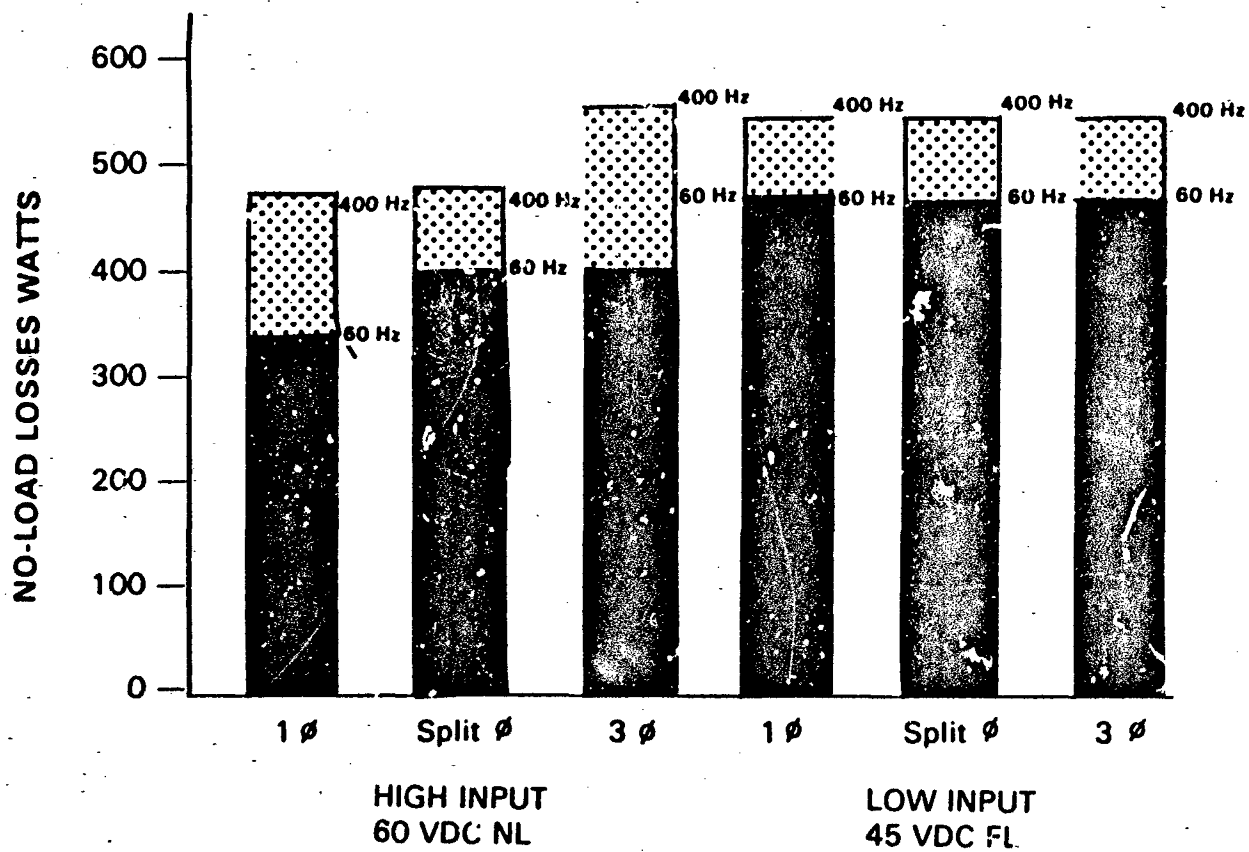
In actual operation the output current is really the rectified output current which can have high peak and valley ratios with respect to the effective direct current value. The efficiency of the booster varies greatly between the peak current and valley current; therefore, the overall efficiency is less than the maximum at the design point of full load direct current.

The effect of the output current variation on the booster could be reduced with very large filter capacitors but would require large volume and added weight to the unit.

Figure V-1 indicates that the no-load losses are a function of input voltage, output frequency, and output configurations. At low input voltage the booster losses are dominant and only output frequency affects the losses. As the input voltage increases the booster losses decrease and the effects of output configuration as well as frequency are observed.

These losses indicate that the circulating filter current is large compared to the full load current. The amount of circulating current is a direct result of the multiple frequency output filter design resulting from the system requirements.

MERADCOM 5KW INVERTER
NO-LOAD LOSSES AS A FUNCTION OF INPUT, CONFIGURATION AND FREQUENCY



CONFIGURATION AND INPUT
FIGURE V-1

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SECTION VI
CONCLUSIONS

The basic theory of design of the MERADCOM 5 kW preprototype inverter is capable of meeting the performance objectives. The equipment is ideally flexible in the sense that any one of three modes at 60 Hz or 400 Hz is available by switch selection. This performance is maintained over an input voltage range of 36-60 VDC. The equipment is mechanically rugged and compact, to serve its intended purpose in a relatively hostile environment.

The system does suffer from limitations. It tends to be prone to electrical noise, particularly in the PWM section. Adequate shielding will minimize this effect. Occasional circuit failures may be eliminated through minor changes in the inverter stage design. Increased current capability for the inverter power switches is required. Lack of external test points and/or BITE makes fault analysis difficult. The Power Supply and the cooling approach need improvements.

The current MERADCOM design is a blend of digital and analog techniques--the result of an effort to obtain the best performance from the least number of discrete components. Future systems of this type may contain some form of microprocessor of a relatively passive type. The PWM technique lends well to this advanced digital technology, and naturally provides a number of side benefits without added complexity i.e., BITE, self monitoring and fault diagnosis.

APPENDIX A

During the month of September 1982, the MERADCOM inverter distortion problem was investigated. The problem was said to be in the feedback system which was used exclusively to improve the waveform. Various feedback techniques had been tried over the previous month(s) with no apparent success. The problem seemed to be with the low order harmonics, i.e., the third, fifth seventh, etc.

The feedback system that was then being used was an arrangement whereby the output of the actual inverter was compared to a "mock" inverter output. The mock inverter output was derived from a low power (signal level) inverter made up of operational amplifiers, etc. This mock inverter was theorized to be free of any of the low order harmonics which were caused by the inverter switching bridge, the filter or any other possible sources of harmonics. The difference between the two sinewave outputs of the real and mock inverters was applied in a negative sense to the inverter reference. This is a promising scheme since the feedback seemingly accounts for all the phase shifts through the filter.

In fact, the phase shifts through the filter can still cause problems. That is the output voltage of the inverter is, in terms of time, phase shifted 180 degrees through the filter for frequencies above the filter resonant point. Since the filter is tuned to approximately 3.5 times the 400 hertz fundamental, the fifth, seventh, etc. will all be 180 degrees phase shifted. According to control theory, the system will be unstable for loop gains higher than 1.0 at the frequency in question (the fifth harmonic, 2000 hertz). It is for this reason that rate feedback alias jerk feedback, is so commonly used. In rate feedback systems the first derivative of the output voltage is sensed by sensing the output filter capacitor current. This reduces the phase angle buildup through the filter to 90 degrees. The system then has a chance of being stable, so long as other system components do not introduce 90 degrees or more while the gain is above 1.0.

With this information in hand, the MERADCOM feedback was modified to incorporate rate feedback. The results were, unexpectedly, not good. Although the system was not unstable, it did not seem to be fixing up the waveform. At this point a thorough investigation was made with the spectrum analyzer to determine the cause of the unexpected reaction.

This investigation confirmed the fact that the source of the unwanted harmonics was the inverter bridge. The specific problem was the inability of the bridge to deliver voltages near zero amplitude. This mechanism arises from the fact that the actual switching time of a particular transistor can be less than the allowed underlap time. When this situation arises, the transistor pole output voltage will be determined by another variable, usually the pole current. That is, the pole current will force the pole voltage to either + or - link voltage depending on the polarity of the current. The result is either a switch early or a switch late condition. The switch early condition occurs when the pole load is power consuming and the pole voltage will change when the off going transistor turns off. The switch late

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condition occurs when the pole load is power sourcing and the pole voltage will remain where it is, past the point of the off going transistor until the oncoming turns on and forces the voltage to change. In either case the pole has a definite voltage but the timing is somewhat off. This problem can usually be corrected with appropriate feedback as discussed above.

If, however, the pole load (current) is near zero, then the pole voltage may not be forced to either + or - link voltage. This condition is referred to as the uncertain condition since it is neither of the desired voltages, link + or -. The result is that no output voltage is available when the pole current is near zero. The level of severity of this problem is related to the amount of uncertain time in the power pole switch design. In the MERADCOM inverter this time amounts to as much as 9 percent of the switching repetition rate. This is based on the worst case assumption that the uncertainty time is equal to the underlap time of 12 microseconds.

It is difficult if not impossible to create a feedback circuit that will correct for the inverter's inability to produce voltage below 9 percent. It would take infinite feedback gain to compensate for the zero feedforward gain of the inverter below the 9 percent voltage level.

The same switching frequency is used in the MERDACOM inverter for both the 400 hertz and the 60 hertz modes. The distortion problem is worse for the 60 hertz mode because the near zero crossover voltage is made up of many switch periods rather than only one or two for the 400 hertz case. The operating frequency of the 400 hertz system is closer to the filter resonant frequency thereby allowing the filter to carry it through the zero crossings with less distortion. In the 60 hertz case the filter has little effect near the zero crossing and the full effects of the missing voltage are more apparent to both the eye and the distortion measuring equipment.

The only solution, then, appears to be to modify the underlap approach such that the uncertainty time is either reduced or eliminated. Suggested approaches follow:

1. Reduce underlap time to 6 microseconds or less. This would require faster turn off circuits, such as a 2 diode CCFT driver arrangement and perhaps other changes.

2. Eliminate underlap altogether by using a full time interlock circuit.

3. Reduce switching frequency.

Another change which may help distortion somewhat, although it is not related to the uncertainty problem, is to control the DC content of both poles of each phase to the link mid point rather than one pole to the other. This was found to be essential to keep even harmonics to acceptable levels on VSCF inverters.